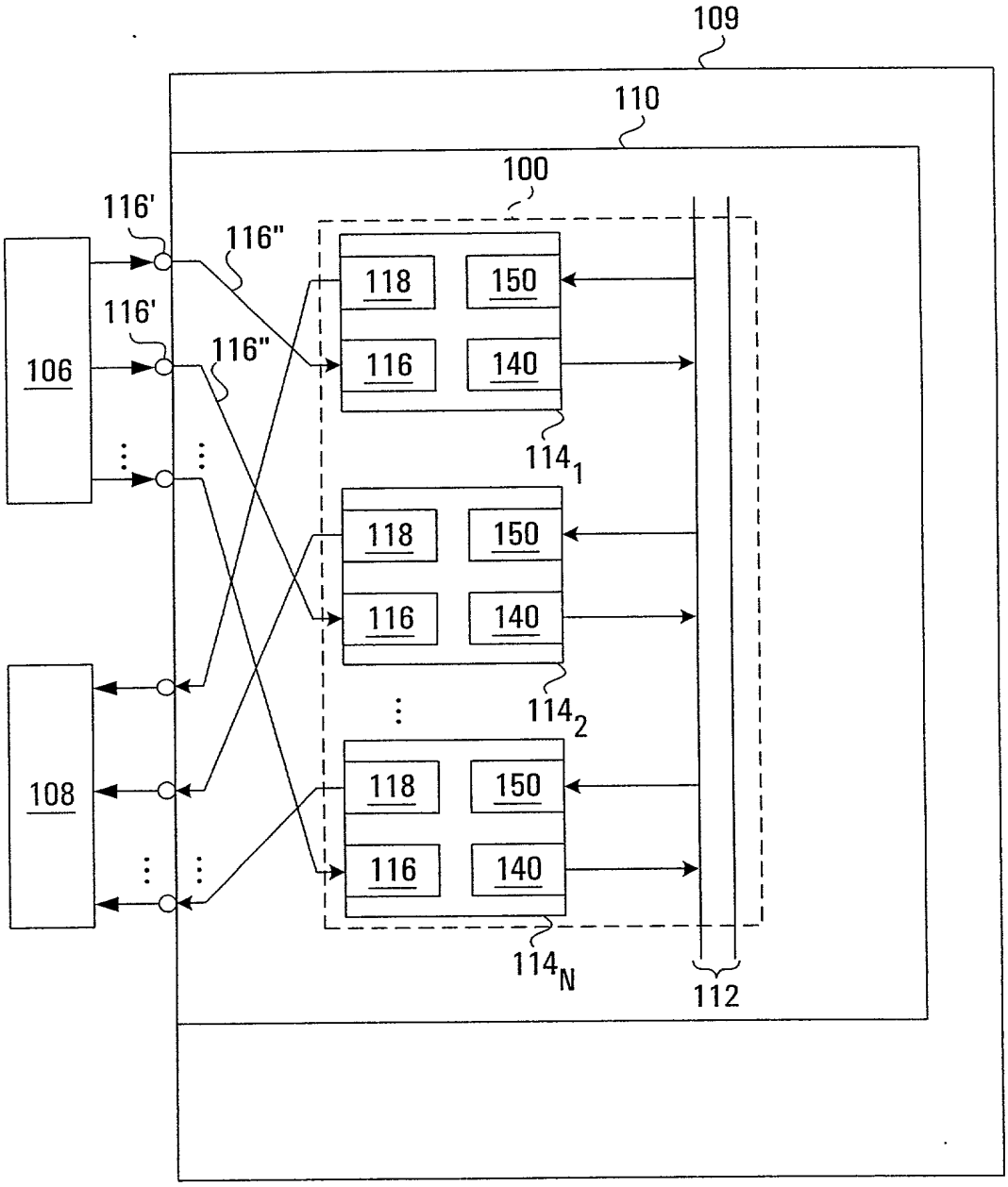

109
110
100
116'
116"
116'
116"
106
118
150
116
140
114_1
118
150
116
140
114_2
108
118
150
116
140
114_N
112

FIG. 1

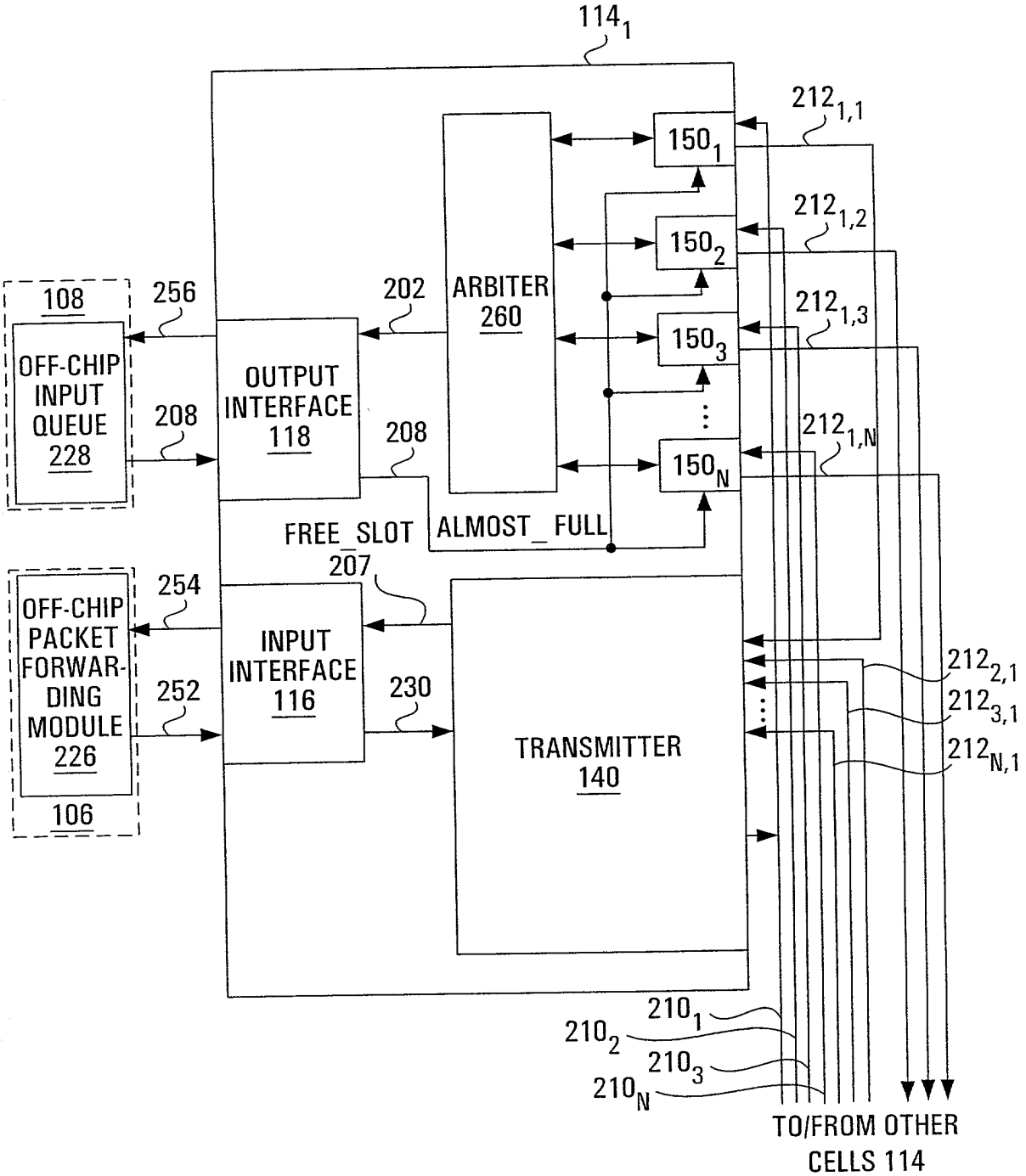

114_1
$212_{1,1}$
150_1
$212_{1,2}$
150_2
ARBITER
260
202
256
108
OFF-CHIP
INPUT
QUEUE
228
OUTPUT
INTERFACE
118
208
208
$212_{1,3}$
150_3
$212_{1,N}$
150_N
FREE_SLOT
ALMOST_FULL
207
254
OFF-CHIP
PACKET
FORWAR-
DING
MODULE
226
106
INPUT
INTERFACE
116
252
230
TRANSMITTER
140
$212_{2,1}$
$212_{3,1}$
$212_{N,1}$
210_1
210_2
210_3
210_N
TO/FROM OTHER
CELLS 114

FIG. 2

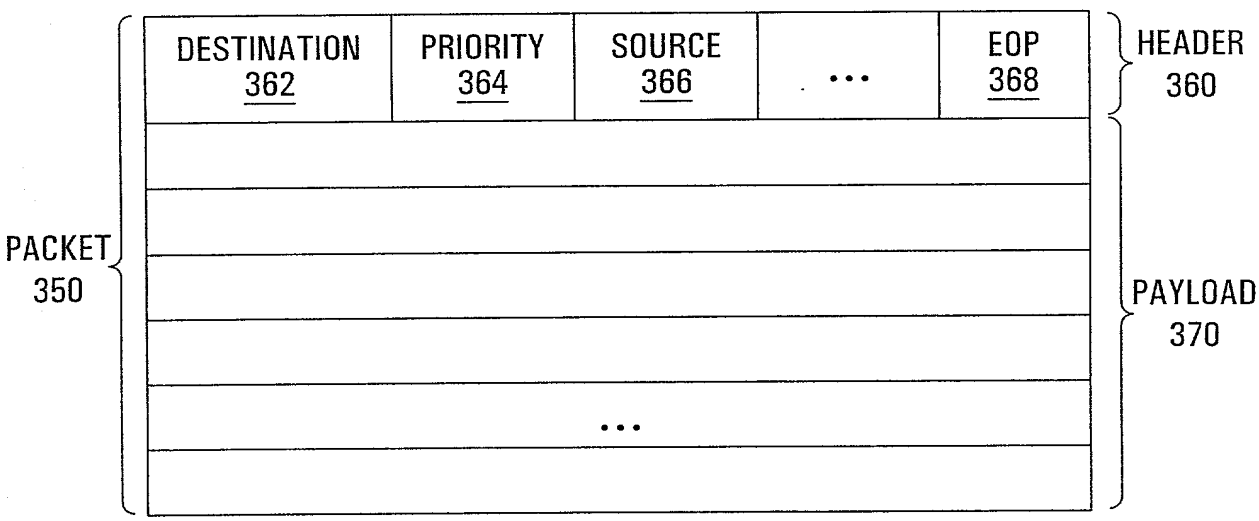

DESTINATION
362
PRIORITY
364
SOURCE
366
...
EOP
368
HEADER
360
PACKET
350
PAYLOAD
370
...

FIG. 3

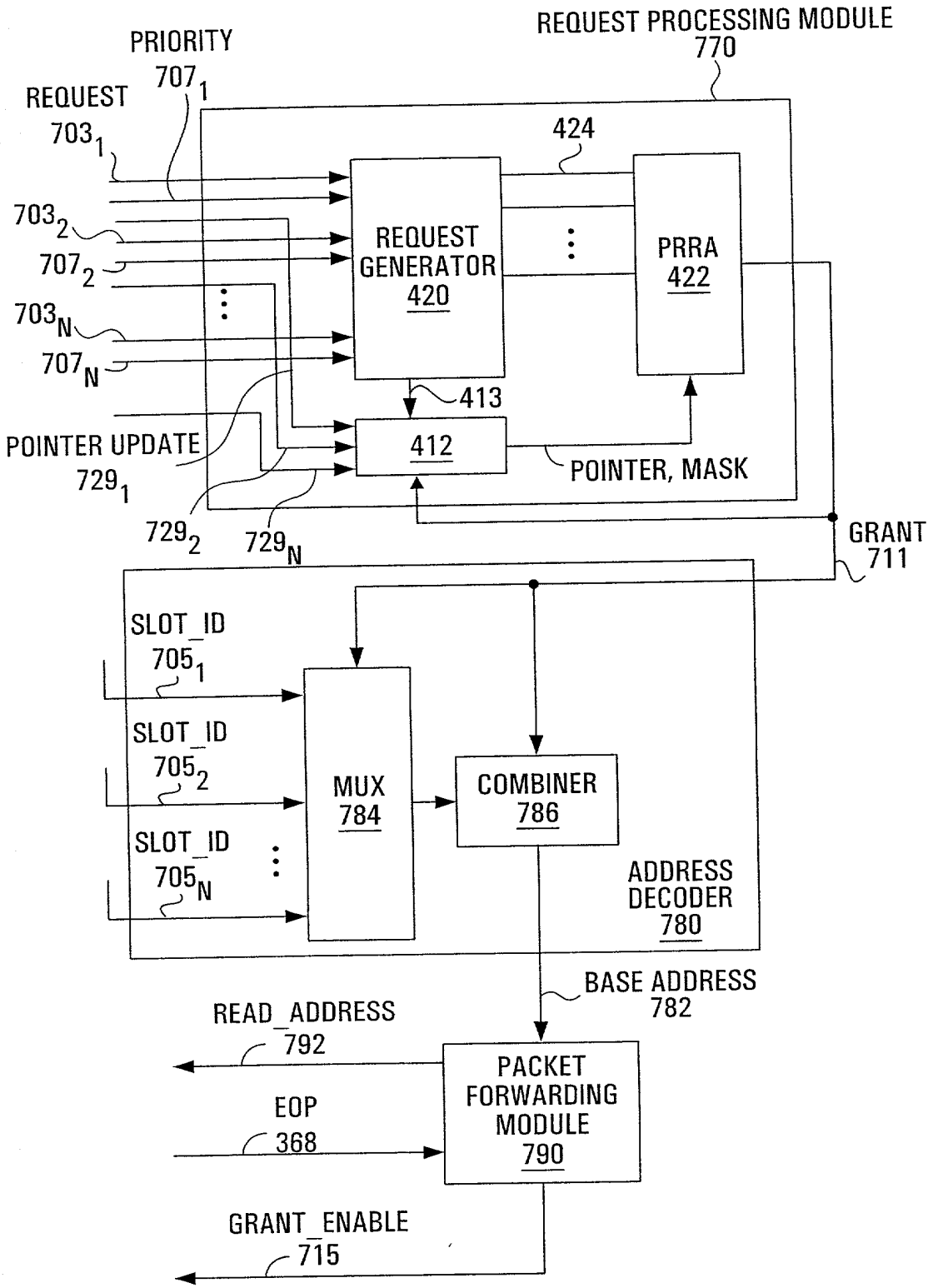

REQUEST PROCESSING MODULE
770
PRIORITY
707_1
REQUEST
703_1
424
703_2
707_2
REQUEST GENERATOR
420
PRRA
422
703_N
707_N
413
POINTER UPDATE
729_1
412
POINTER, MASK
729_2
729_N
GRANT
711
SLOT_ID
705_1
SLOT_ID
705_2
SLOT_ID
705_N
MUX
784
COMBINER
786
ADDRESS DECODER
780
BASE ADDRESS
782
READ_ADDRESS
792
PACKET FORWARDING MODULE
790
EOP
368
GRANT_ENABLE
715

FIG. 4

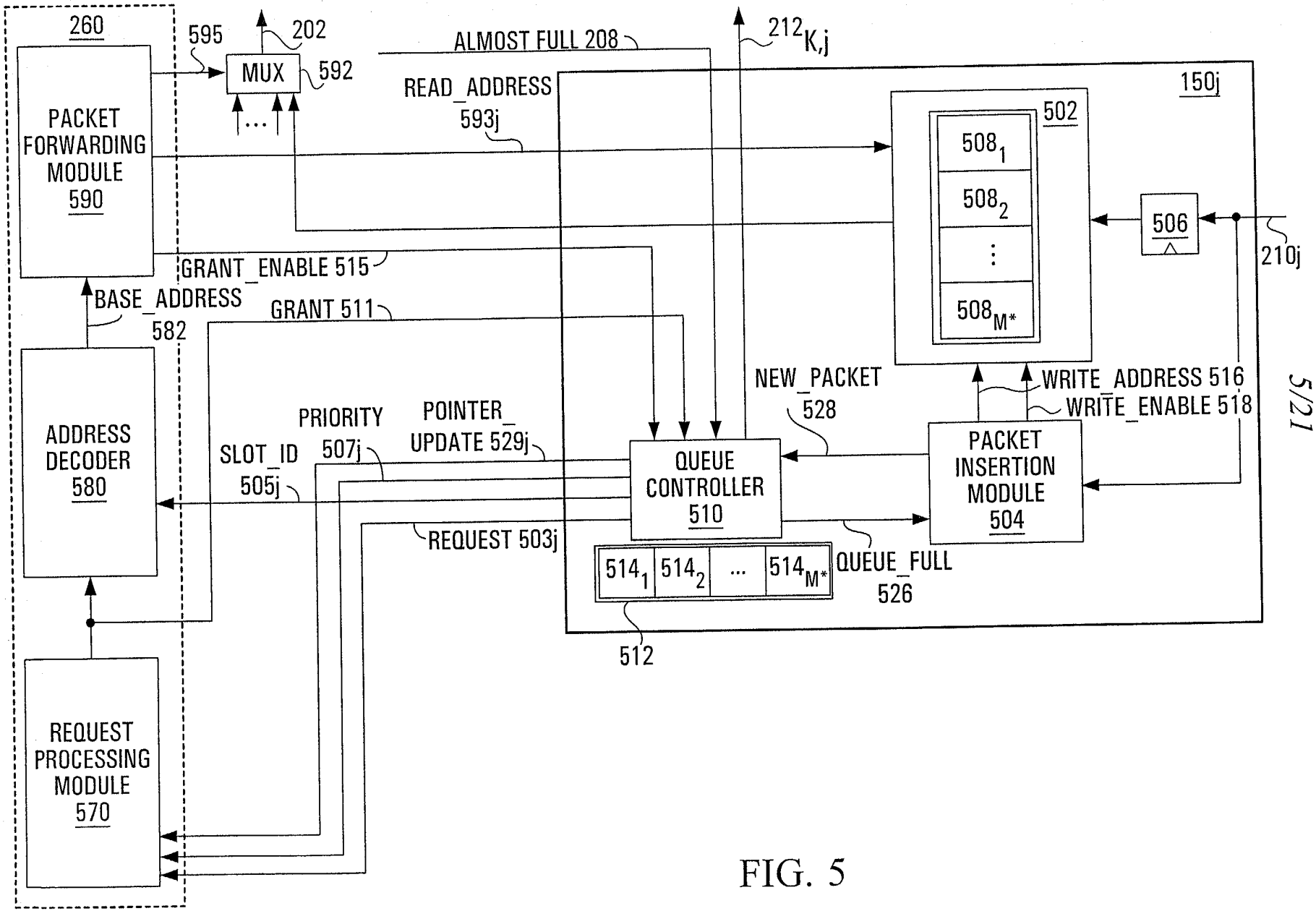


FIG. 5

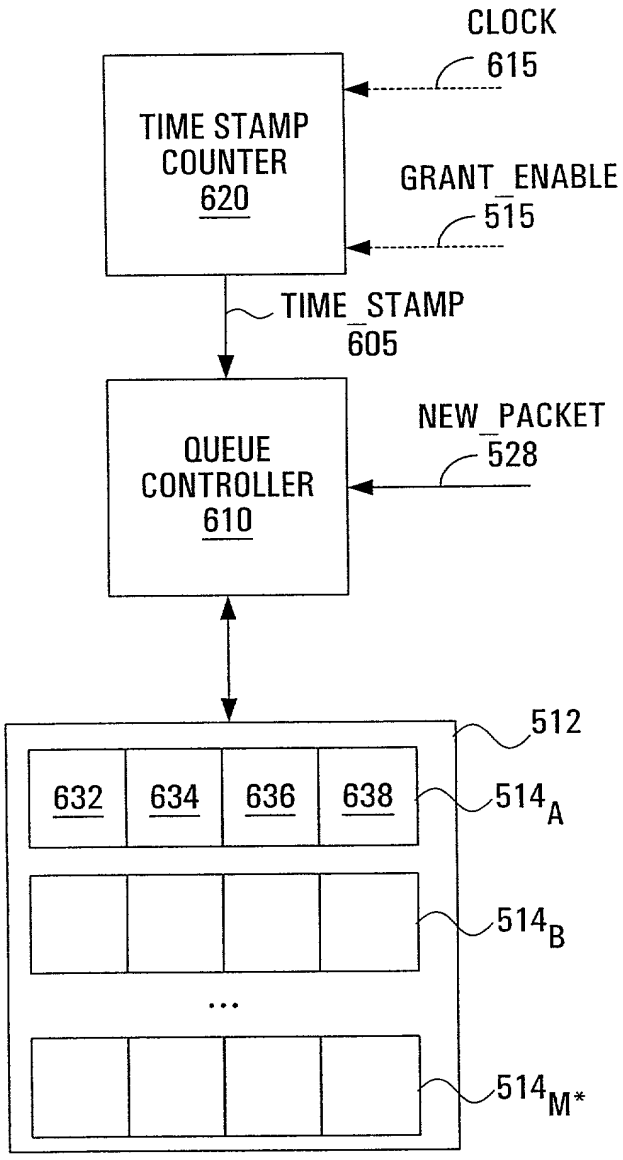

CLOCK
615
TIME STAMP COUNTER
620
GRANT_ENABLE
515
TIME_STAMP
605
QUEUE CONTROLLER
610
NEW_PACKET
528
512
632
634
636
638
514A
514B
...
514M*

FIG. 6

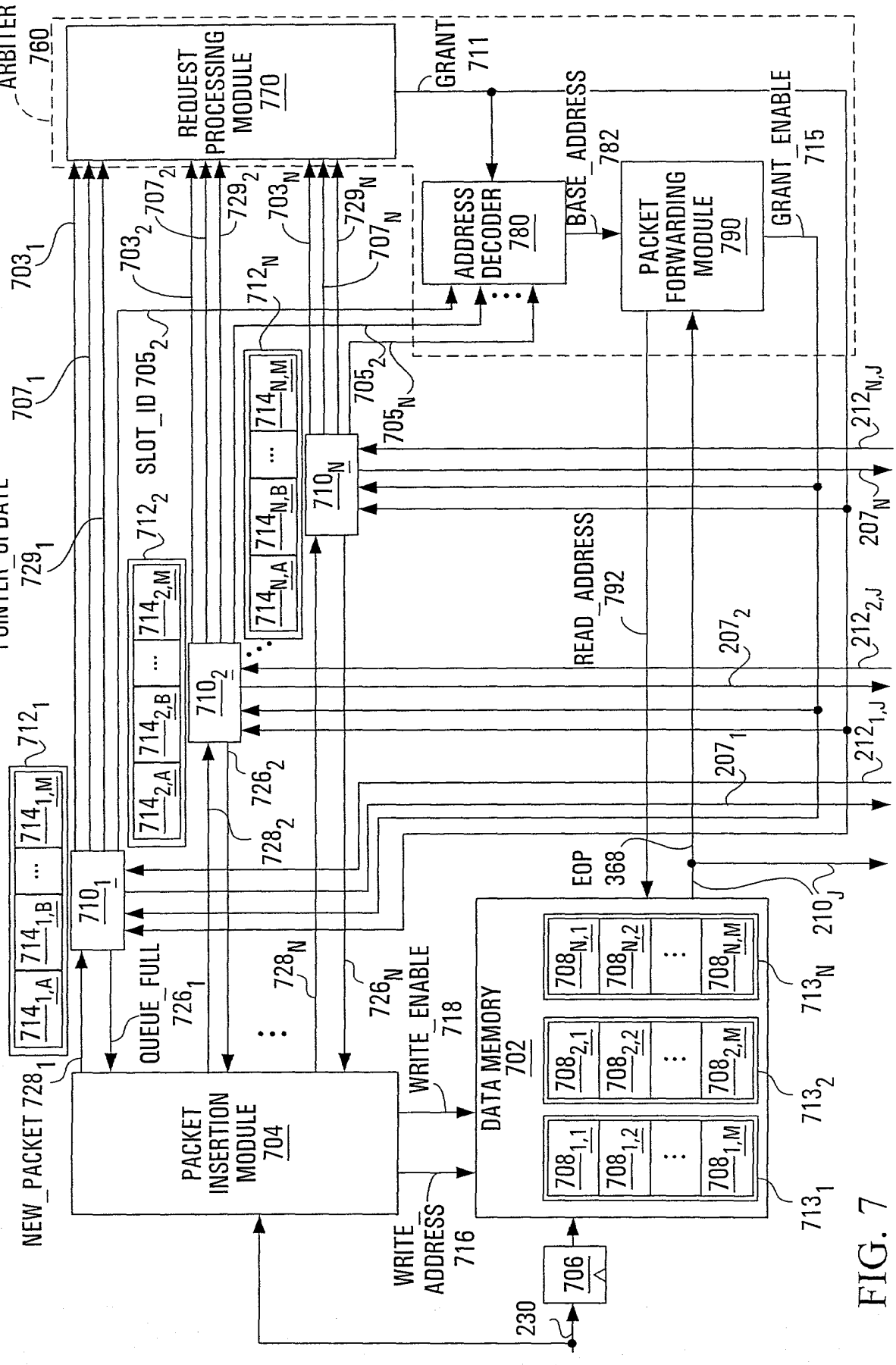

ARBITER 760
REQUEST PROCESSING MODULE 770
GRANT 711
REQUEST 703_1
PRIORITY 707_1
POINTER_UPDATE 729_1
SLOT_ID 705_2
ADDRESS DECODER 780
BASE_ADDRESS 782
PACKET FORWARDING MODULE 790
GRANT_ENABLE 715
READ_ADDRESS 792
NEW_PACKET 728_1
QUEUE_FULL 726_1
WRITE_ENABLE 718
WRITE_ADDRESS 716
PACKET INSERTION MODULE 704
DATA MEMORY 702
EOP 368
706
230

FIG. 7

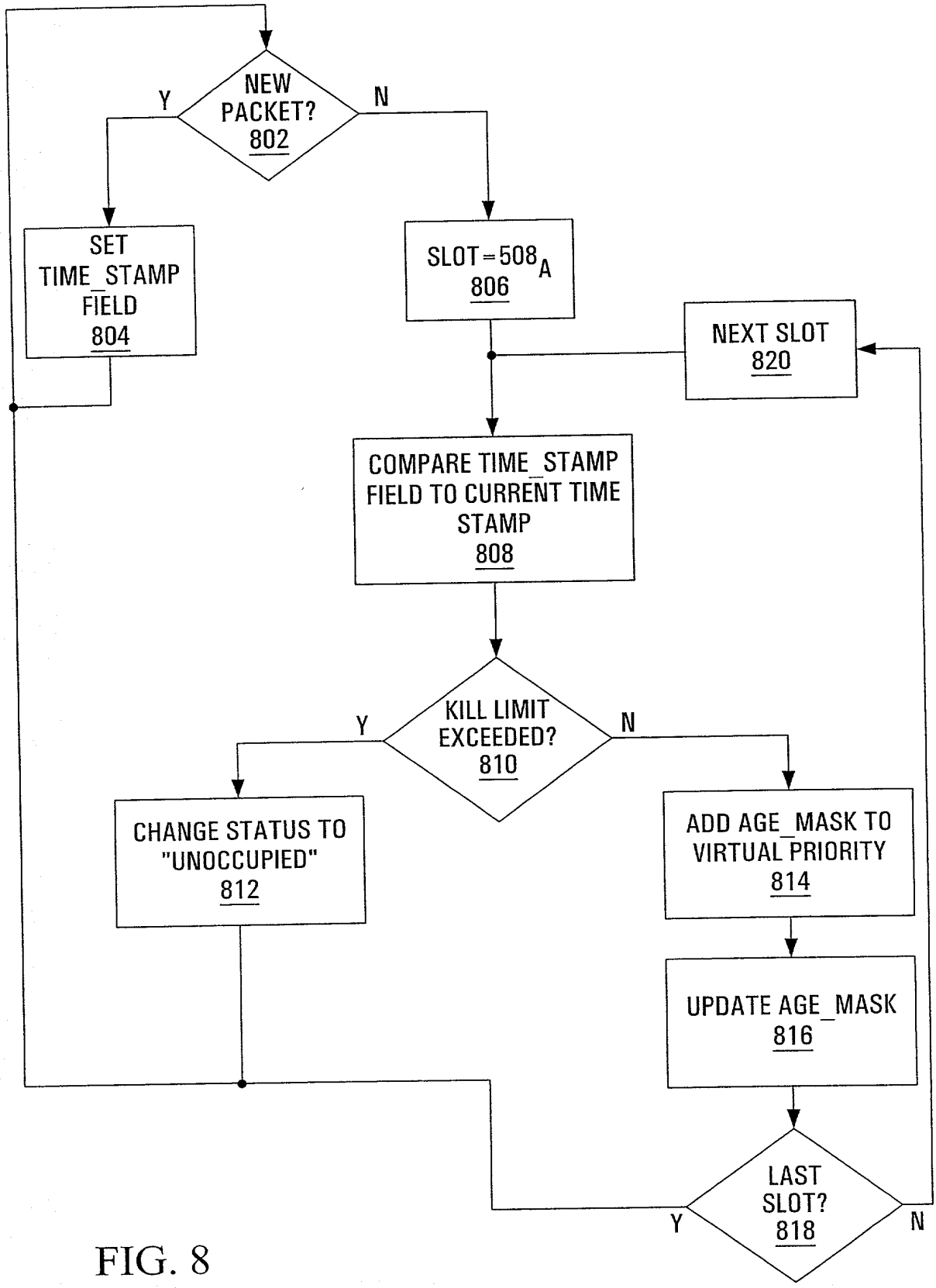

NEW PACKET? 802
Y
N
SET TIME_STAMP FIELD 804
SLOT=508A 806
NEXT SLOT 820
COMPARE TIME_STAMP FIELD TO CURRENT TIME STAMP 808
KILL LIMIT EXCEEDED? 810
Y
N
CHANGE STATUS TO "UNOCCUPIED" 812
ADD AGE_MASK TO VIRTUAL PRIORITY 814
UPDATE AGE_MASK 816
LAST SLOT? 818
Y
N

FIG. 8

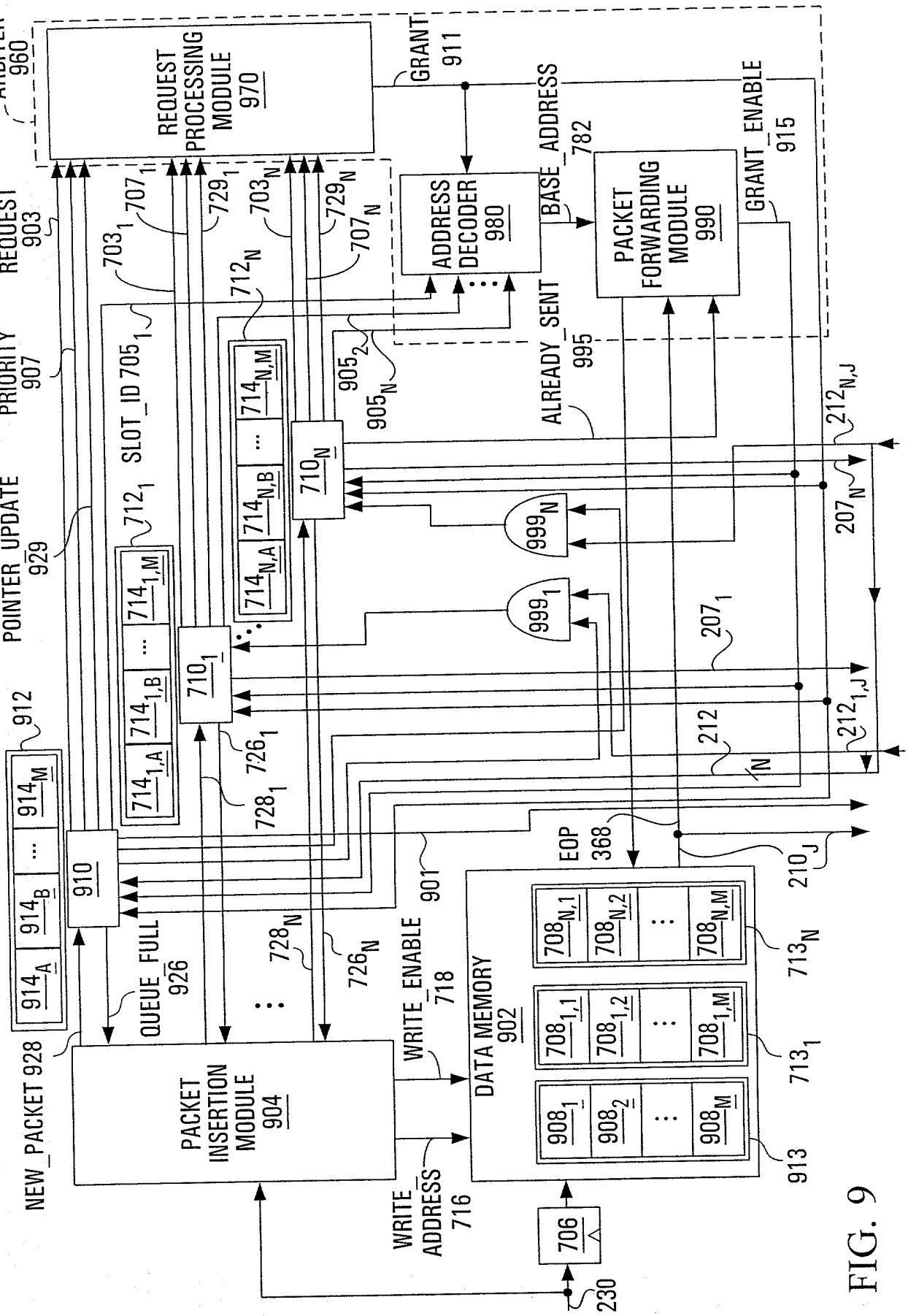

ARBITER 960
REQUEST PROCESSING MODULE 970
GRANT 911
REQUEST 903
PRIORITY 907
POINTER UPDATE 929
SLOT_ID 705$_1$
ADDRESS DECODER 980
BASE_ADDRESS 782
PACKET FORWARDING MODULE 990
GRANT_ENABLE 915
ALREADY_SENT 995
NEW_PACKET 928
QUEUE_FULL 926
PACKET INSERTION MODULE 904
WRITE_ENABLE 718
WRITE_ADDRESS 716
DATA MEMORY 902
EOP 368
706
230
910
912
901
913
N

FIG. 9

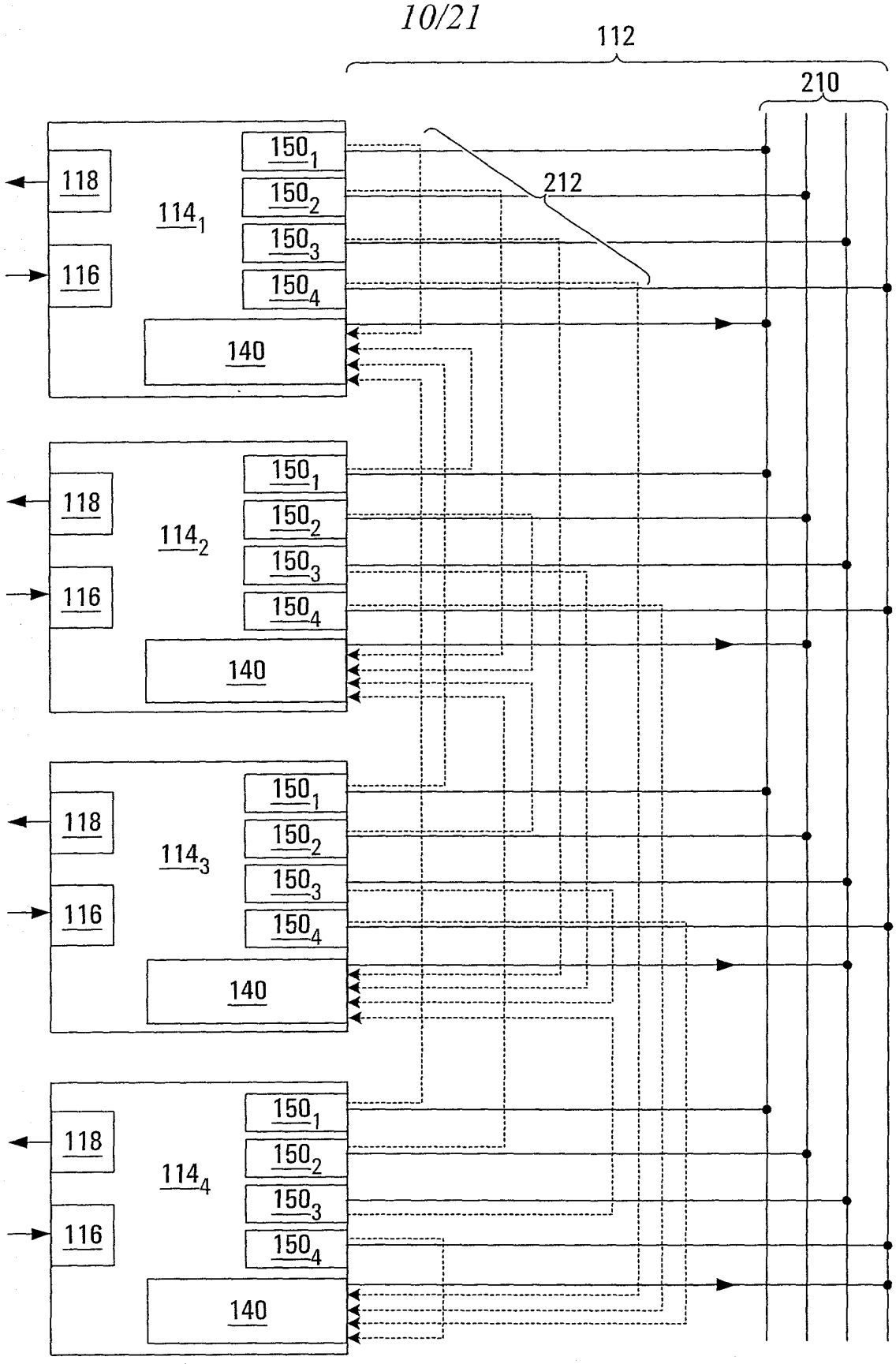

112
210
212
150_1
150_2
150_3
150_4
118
116
140
114_1
114_2
114_3
114_4

FIG. 10

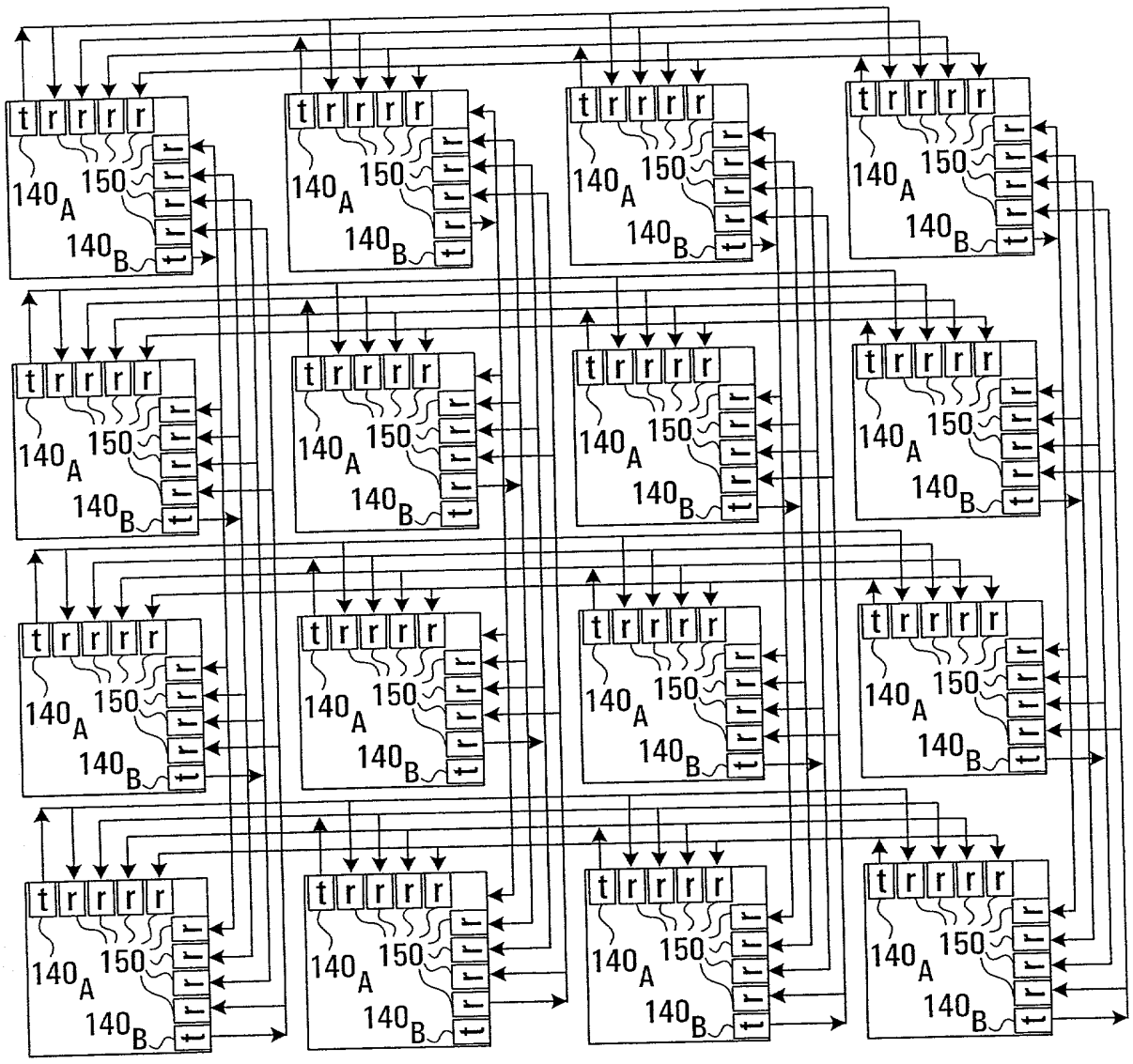


FIG. 11

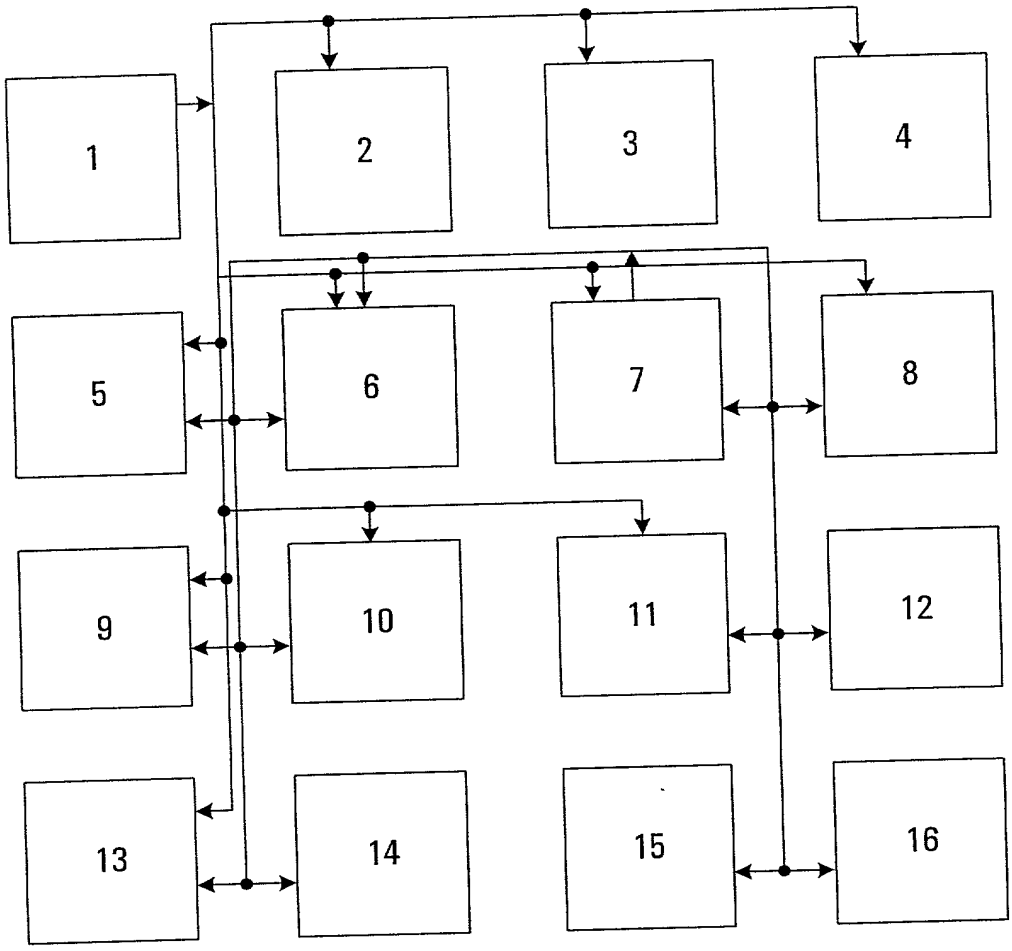


FIG. 12

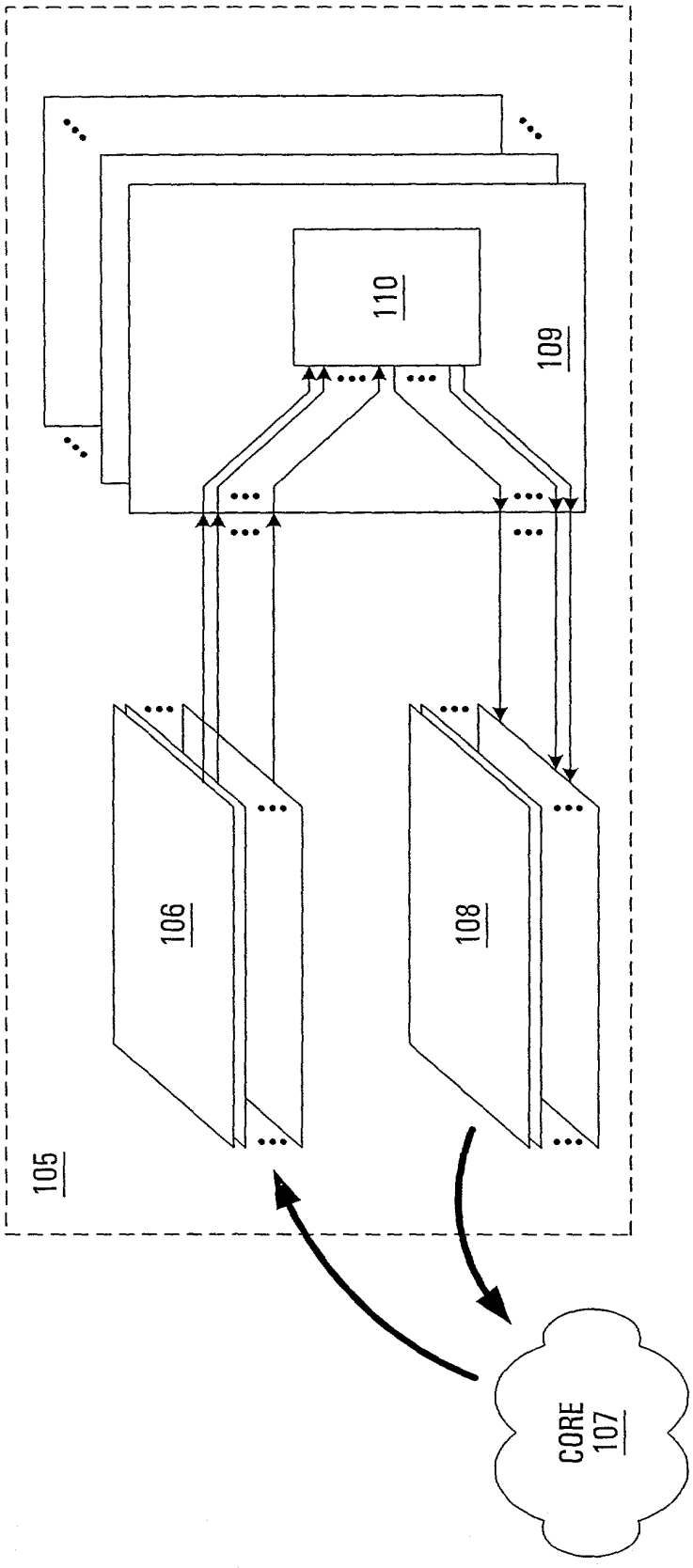


FIG. 13

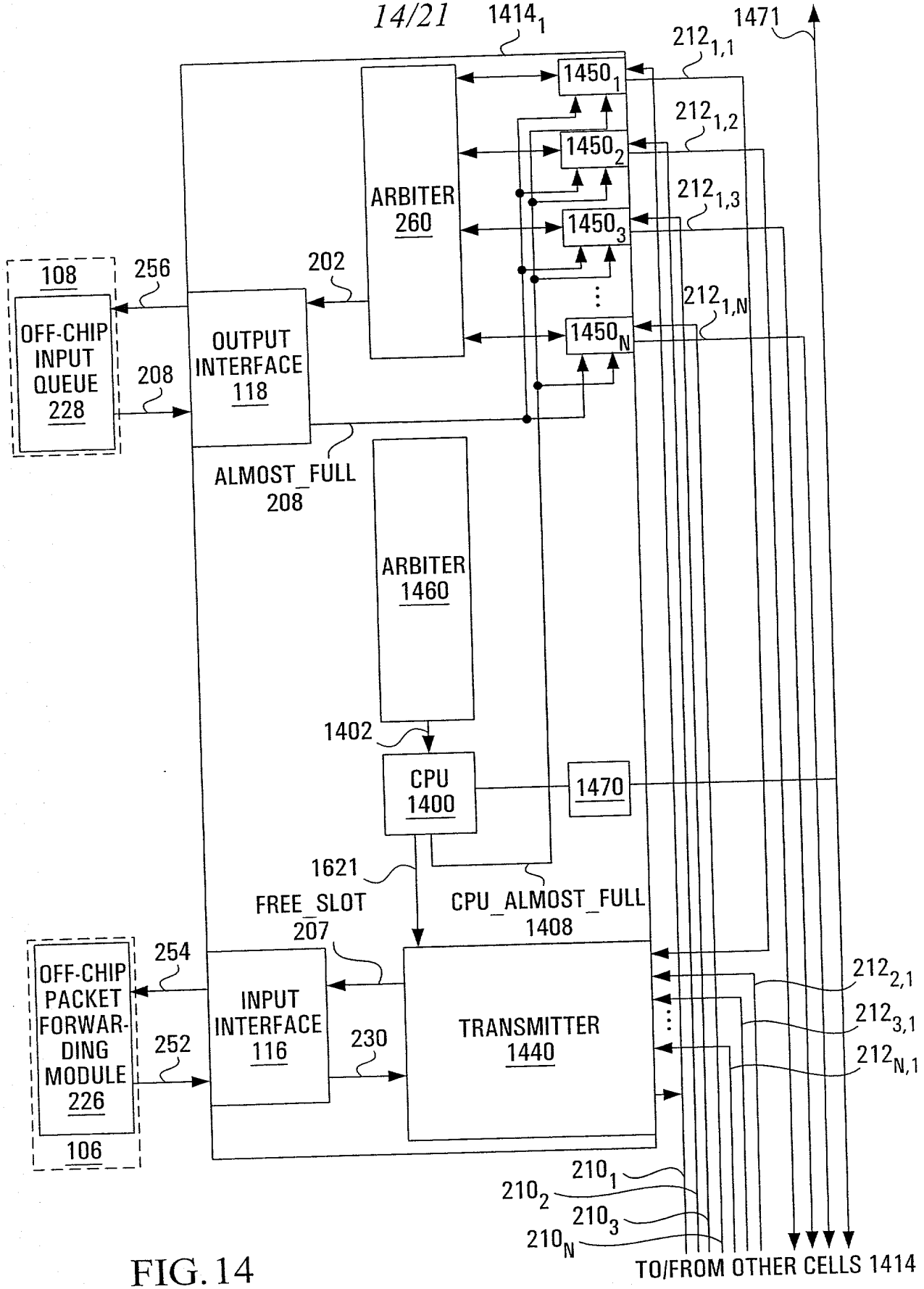

1414_1
1471
212_1,1
1450_1
212_1,2
1450_2
ARBITER 260
212_1,3
1450_3
108
256
202
212_1,N
OFF-CHIP INPUT QUEUE 228
OUTPUT INTERFACE 118
1450_N
208
ALMOST_FULL 208
ARBITER 1460
1402
CPU 1400
1470
1621
FREE_SLOT 207
CPU_ALMOST_FULL 1408
254
212_2,1
OFF-CHIP PACKET FORWAR-DING MODULE 226
INPUT INTERFACE 116
TRANSMITTER 1440
212_3,1
252
230
212_N,1
106
210_1
210_2
210_3
210_N
TO/FROM OTHER CELLS 1414

FIG. 14

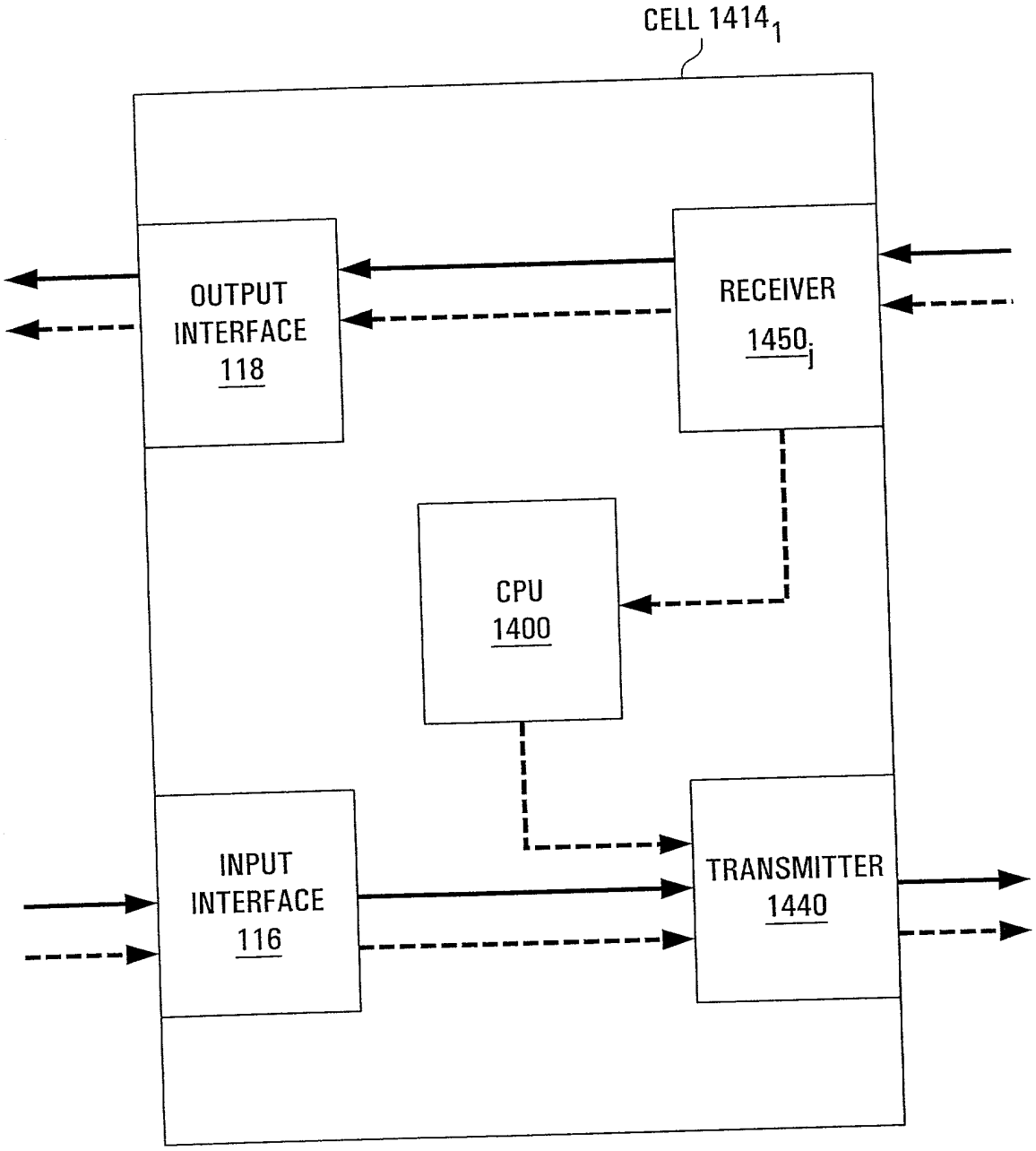


FIG. 15

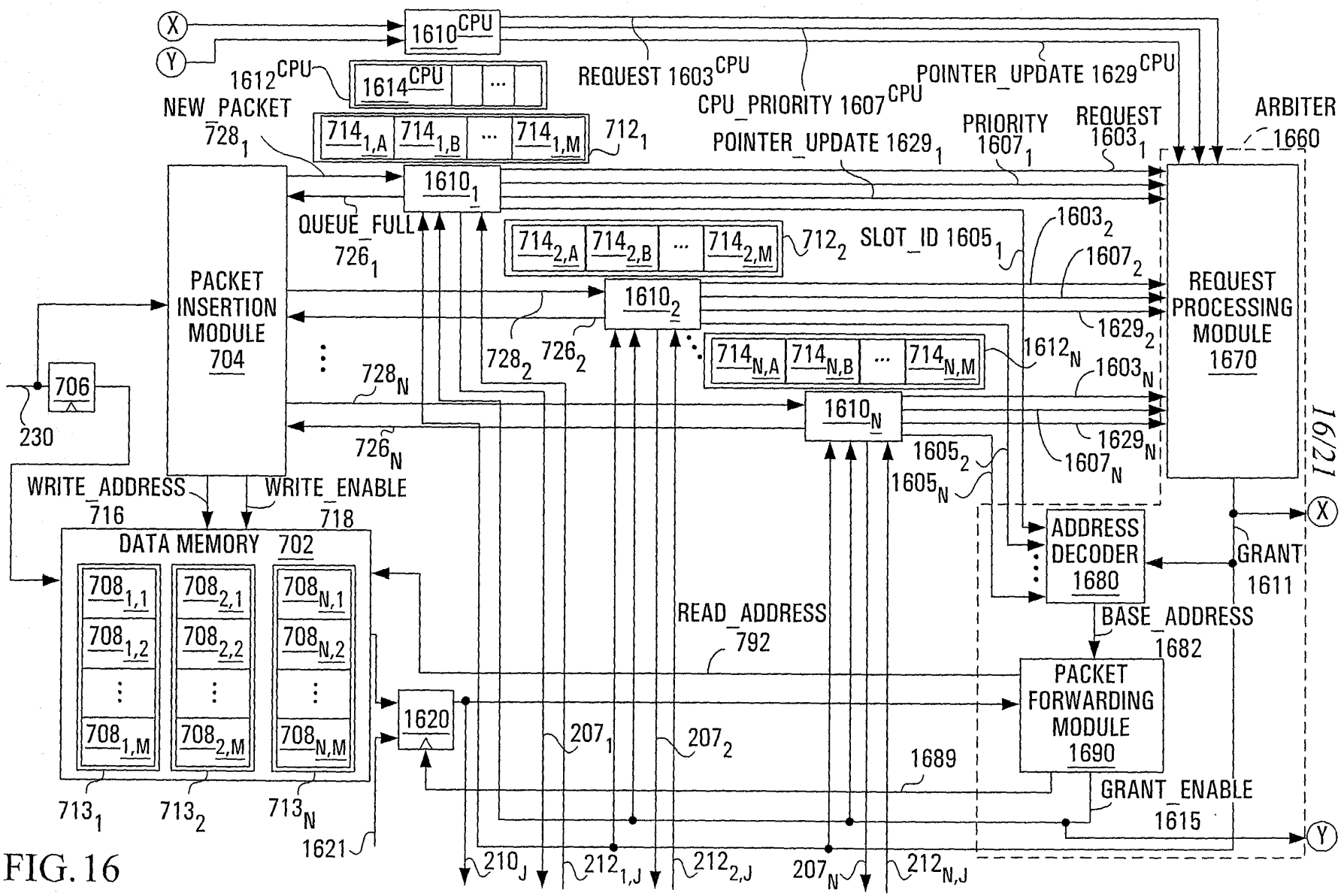

X
Y
1610 CPU
1612 CPU
1614 CPU
REQUEST 1603 CPU
CPU_PRIORITY 1607 CPU
POINTER_UPDATE 1629 CPU
NEW_PACKET 728 1
714 1,A
714 1,B
714 1,M
712 1
POINTER_UPDATE 1629 1
PRIORITY 1607 1
REQUEST 1603 1
ARBITER 1660
1610 1
QUEUE_FULL 726 1
714 2,A
714 2,B
714 2,M
712 2
SLOT_ID 1605 1
1603 2
1607 2
1629 2
PACKET INSERTION MODULE 704
1610 2
REQUEST PROCESSING MODULE 1670
728 2
726 2
714 N,A
714 N,B
714 N,M
1612 N
1603 N
728 N
1610 N
1629 N
706
230
726 N
1607 N
1605 2
1605 N
WRITE_ADDRESS 716
WRITE_ENABLE 718
ADDRESS DECODER 1680
GRANT 1611
DATA MEMORY 702
708 1,1
708 1,2
708 1,M
708 2,1
708 2,2
708 2,M
708 N,1
708 N,2
708 N,M
READ_ADDRESS 792
BASE_ADDRESS 1682
PACKET FORWARDING MODULE 1690
1620
207 1
207 2
1689
GRANT_ENABLE 1615
713 1
713 2
713 N
1621
210 J
212 1,J
212 2,J
207 N
212 N,J
16/21

FIG. 16

FIG. 17A

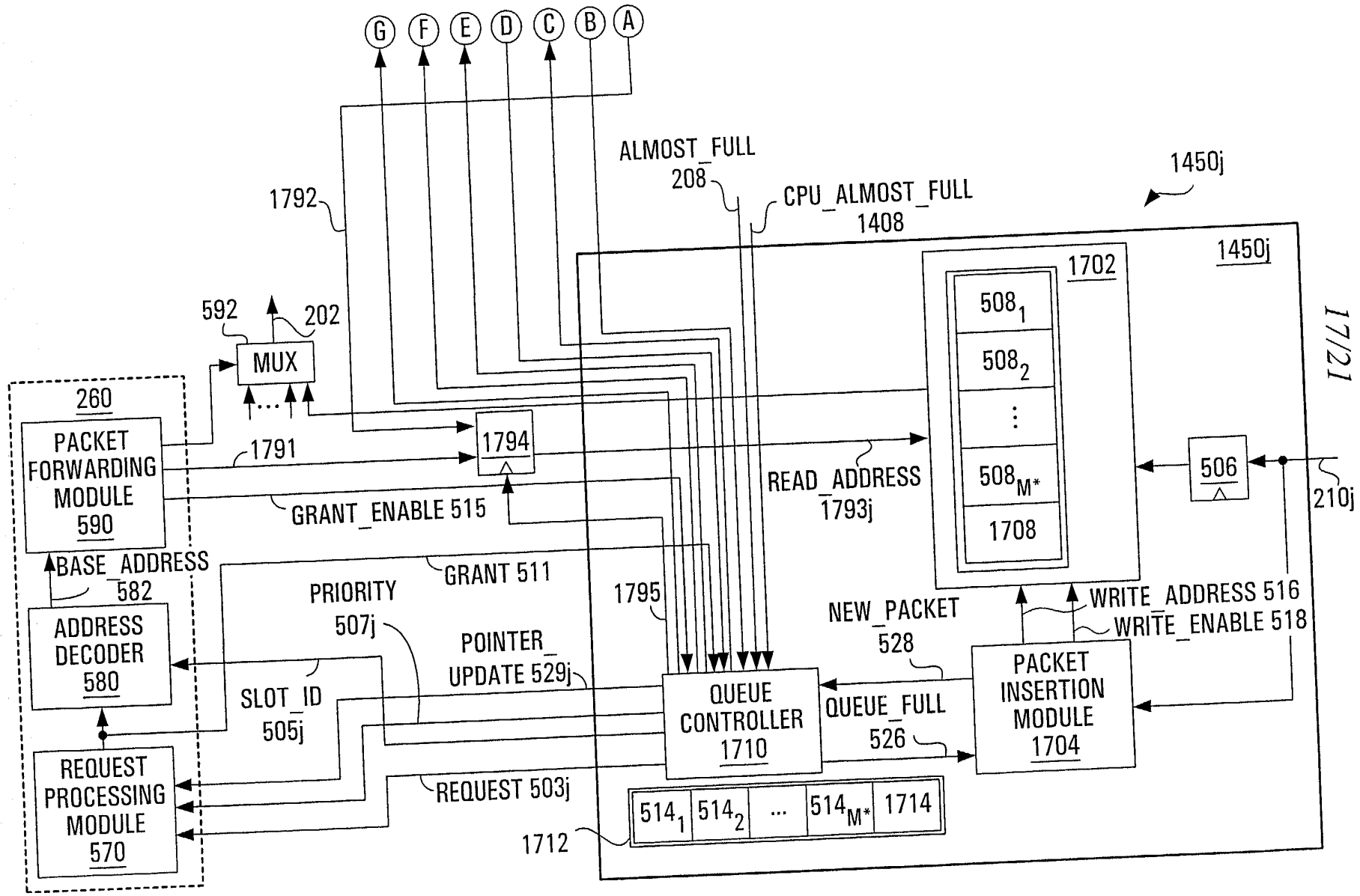
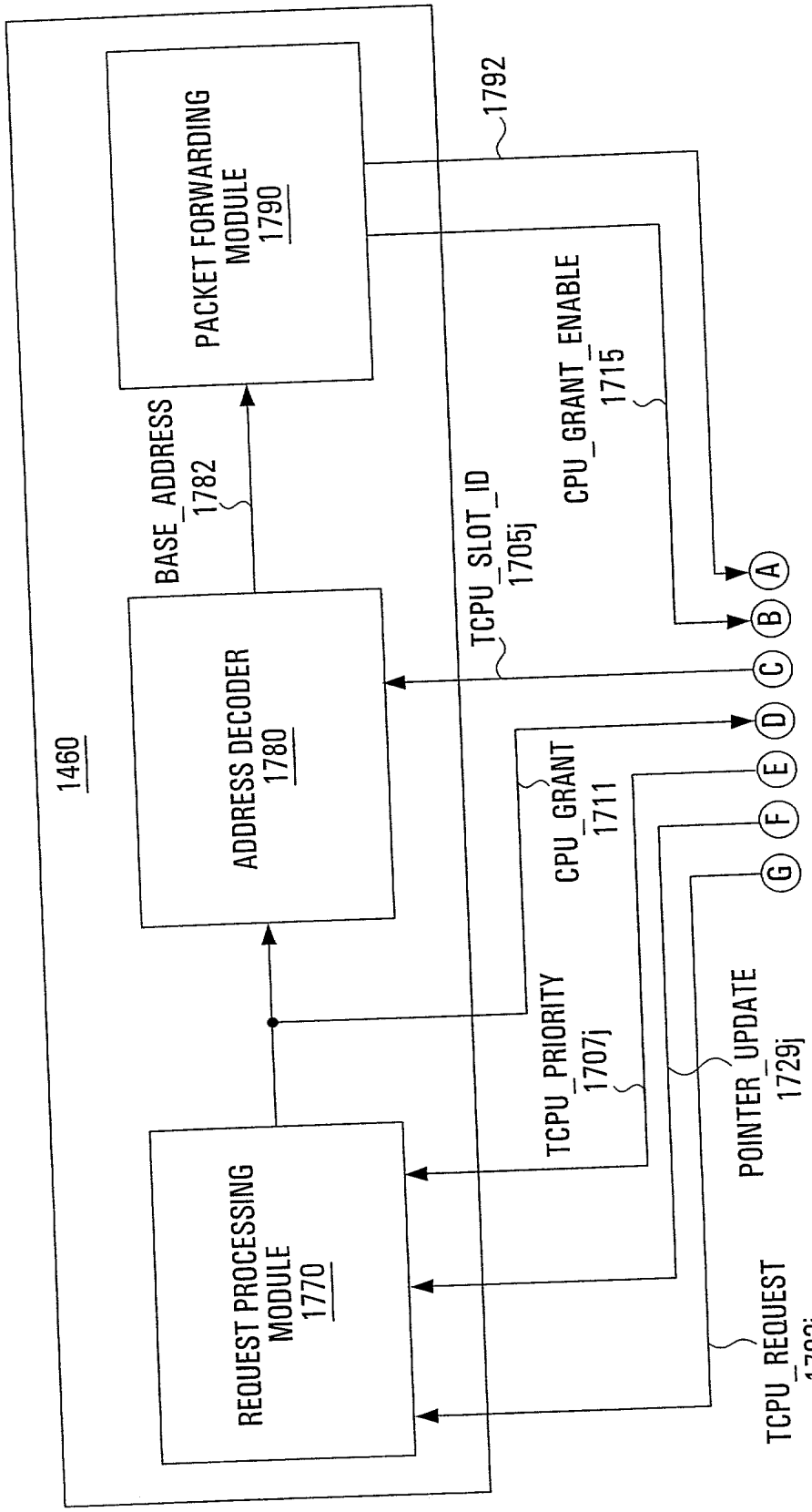

G
F
E
D
C
B
A
ALMOST_FULL
208
CPU_ALMOST_FULL
1408
1450j
1792
1702
1450j
592
202
MUX
260
PACKET FORWARDING MODULE 590
1791
1794
READ_ADDRESS 1793j
506
210j
GRANT_ENABLE 515
BASE_ADDRESS 582
GRANT 511
PRIORITY 507j
1795
NEW_PACKET 528
WRITE_ADDRESS 516
WRITE_ENABLE 518
ADDRESS DECODER 580
POINTER_ UPDATE 529j
SLOT_ID 505j
QUEUE CONTROLLER 1710
QUEUE_FULL 526
PACKET INSERTION MODULE 1704
REQUEST PROCESSING MODULE 570
REQUEST 503j
1712
1714
17/21

FIG. 17B


1460
PACKET FORWARDING MODULE 1790
1792
BASE_ADDRESS 1782
ADDRESS DECODER 1780
TCPU_SLOT_ID 1705j
CPU_GRANT_ENABLE 1715
CPU_GRANT 1711
TCPU_PRIORITY 1707j
POINTER_UPDATE 1729j
REQUEST PROCESSING MODULE 1770
TCPU_REQUEST 1703j
A
B
C
D
E
F
G

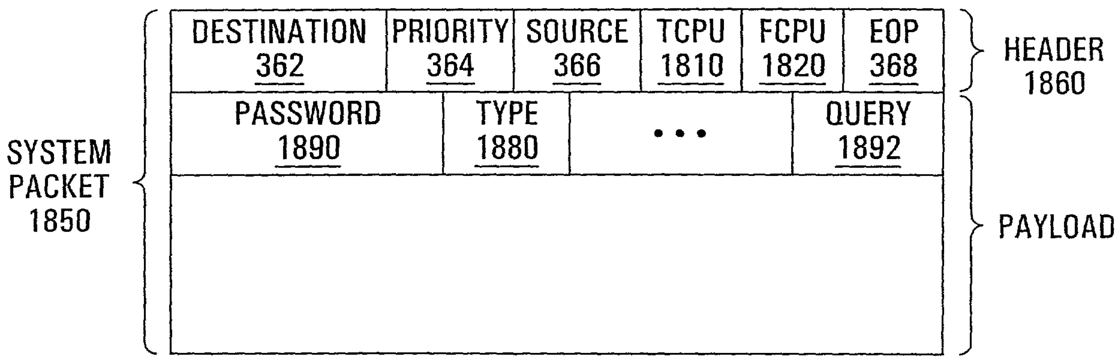


FIG. 18

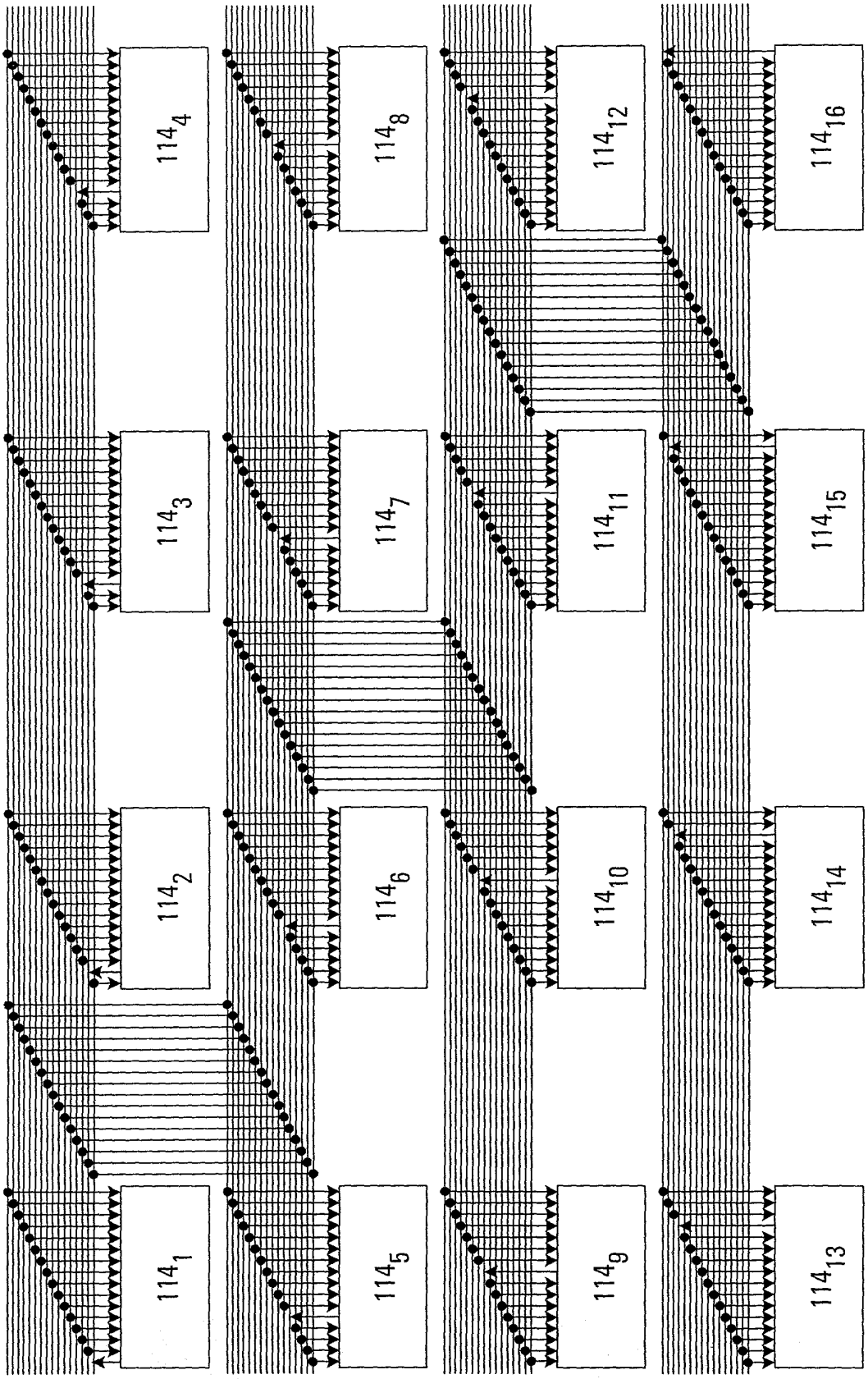

114_1
114_2
114_3
114_4
114_5
114_6
114_7
114_8
114_9
114_{10}
114_{11}
114_{12}
114_{13}
114_{14}
114_{15}
114_{16}

FIG. 19

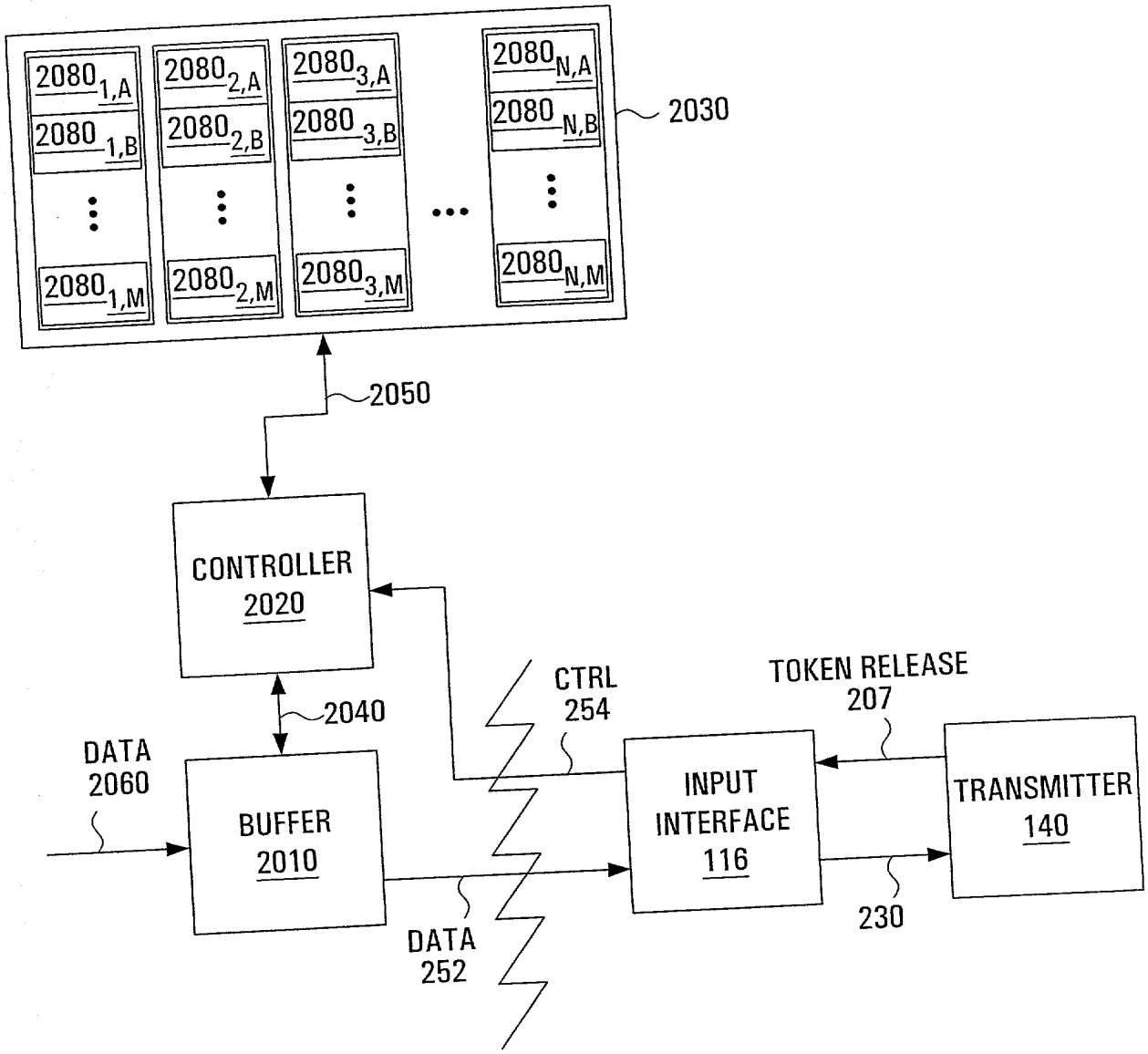

2080 1,A
2080 1,B
2080 1,M
2080 2,A
2080 2,B
2080 2,M
2080 3,A
2080 3,B
2080 3,M
2080 N,A
2080 N,B
2080 N,M
2030
2050
CONTROLLER
2020
2040
DATA
2060
BUFFER
2010
CTRL
254
DATA
252
INPUT
INTERFACE
116
TOKEN RELEASE
207
TRANSMITTER
140
230

FIG. 20